

FIG. 1

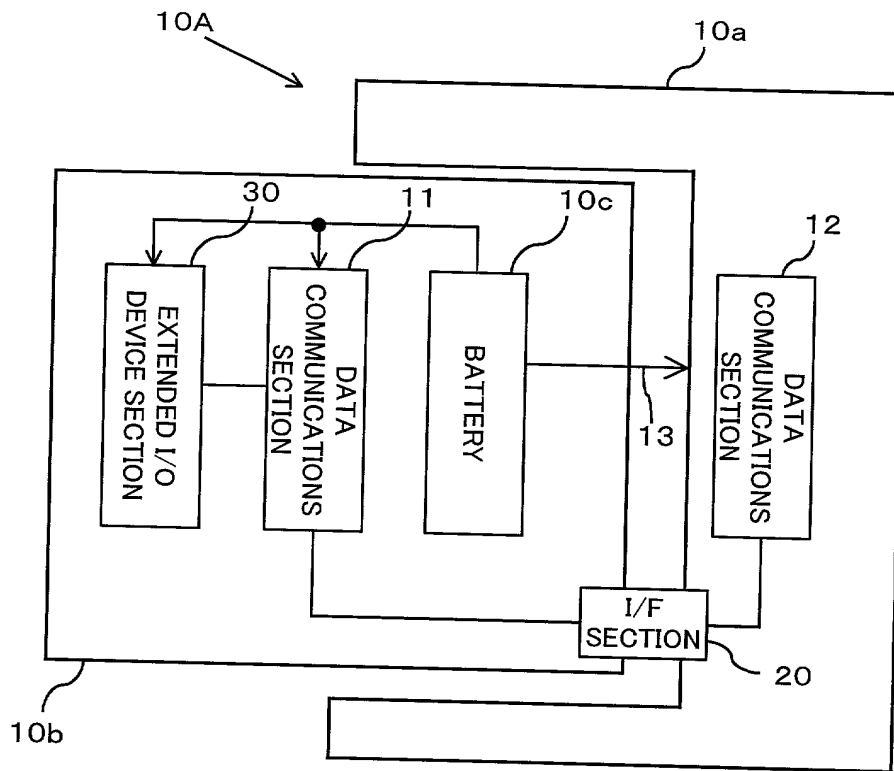
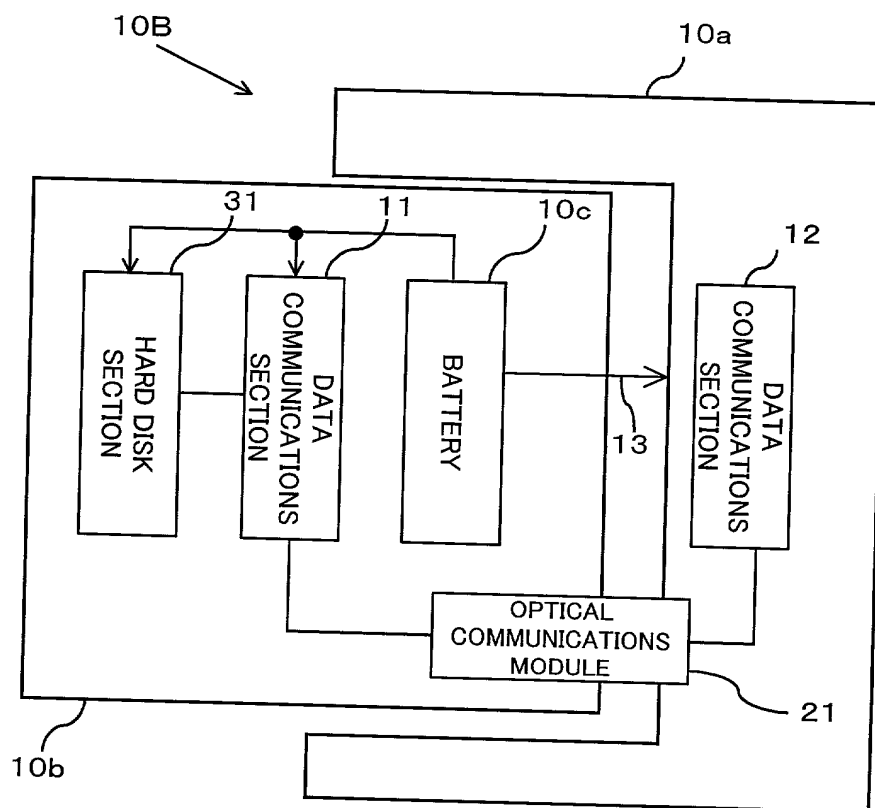
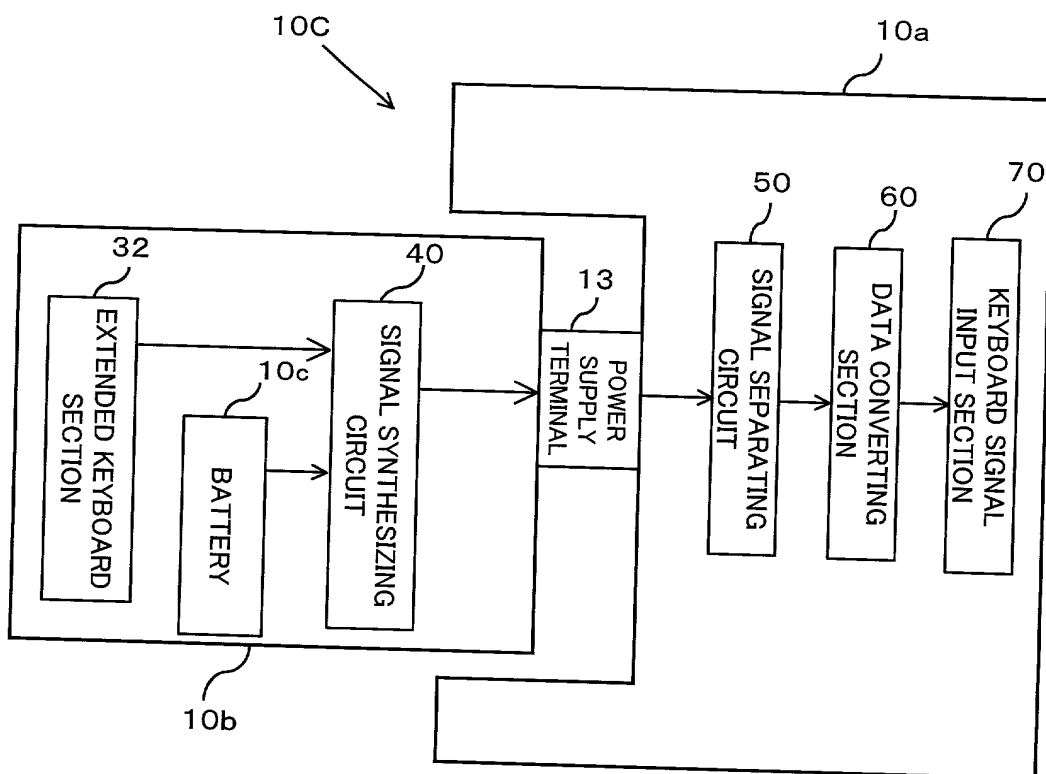


FIG. 2



[illegible]

U.S. Pat. No. 4,111,111, issued June 11, 1978, to the inventor of the present invention.

FIG. 4

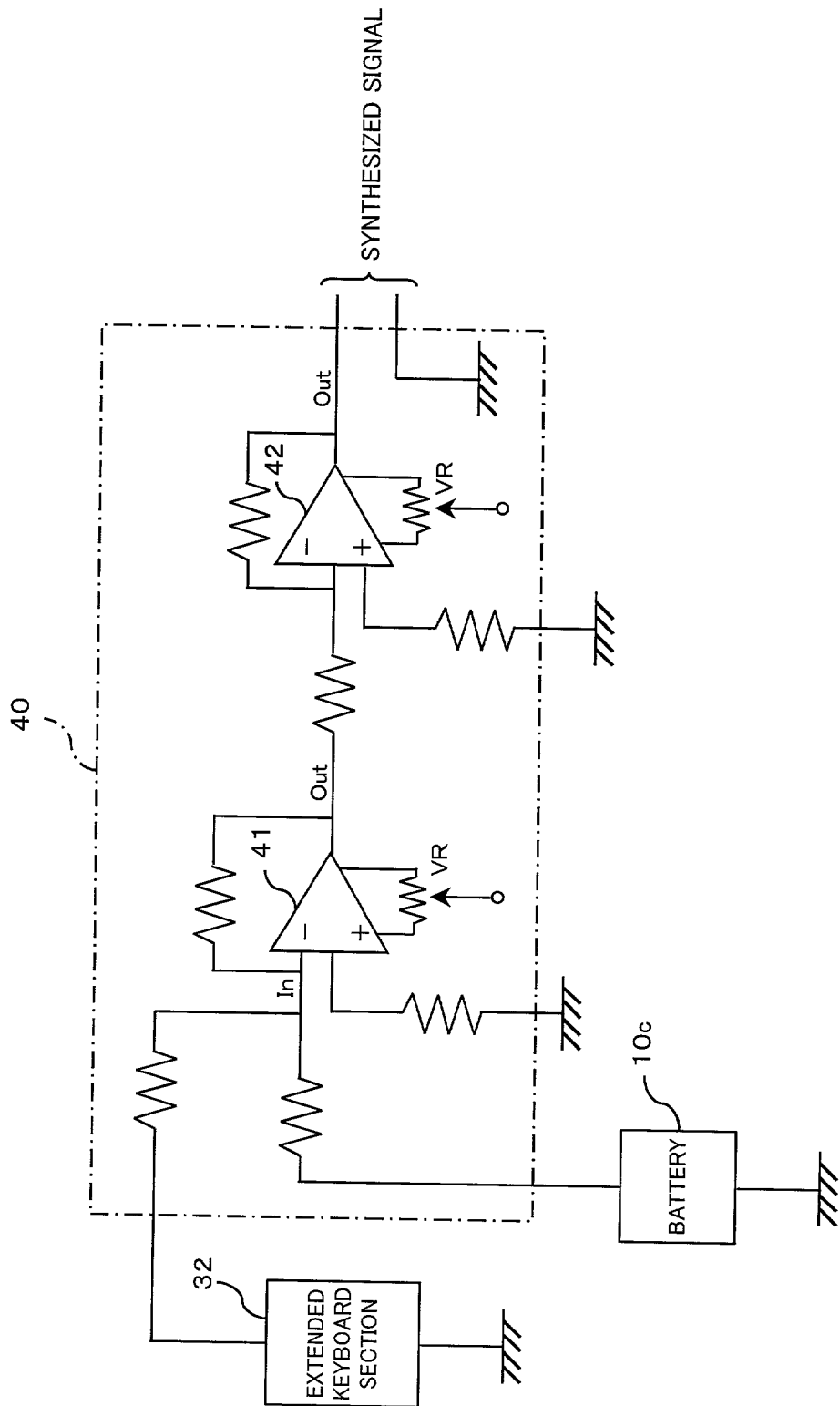


FIG. 5 is a schematic diagram of a circuit 50, which includes two operational amplifiers 51 and 52, a battery 10c, a synthesized signal source, and various resistors and ground connections.

FIG. 5

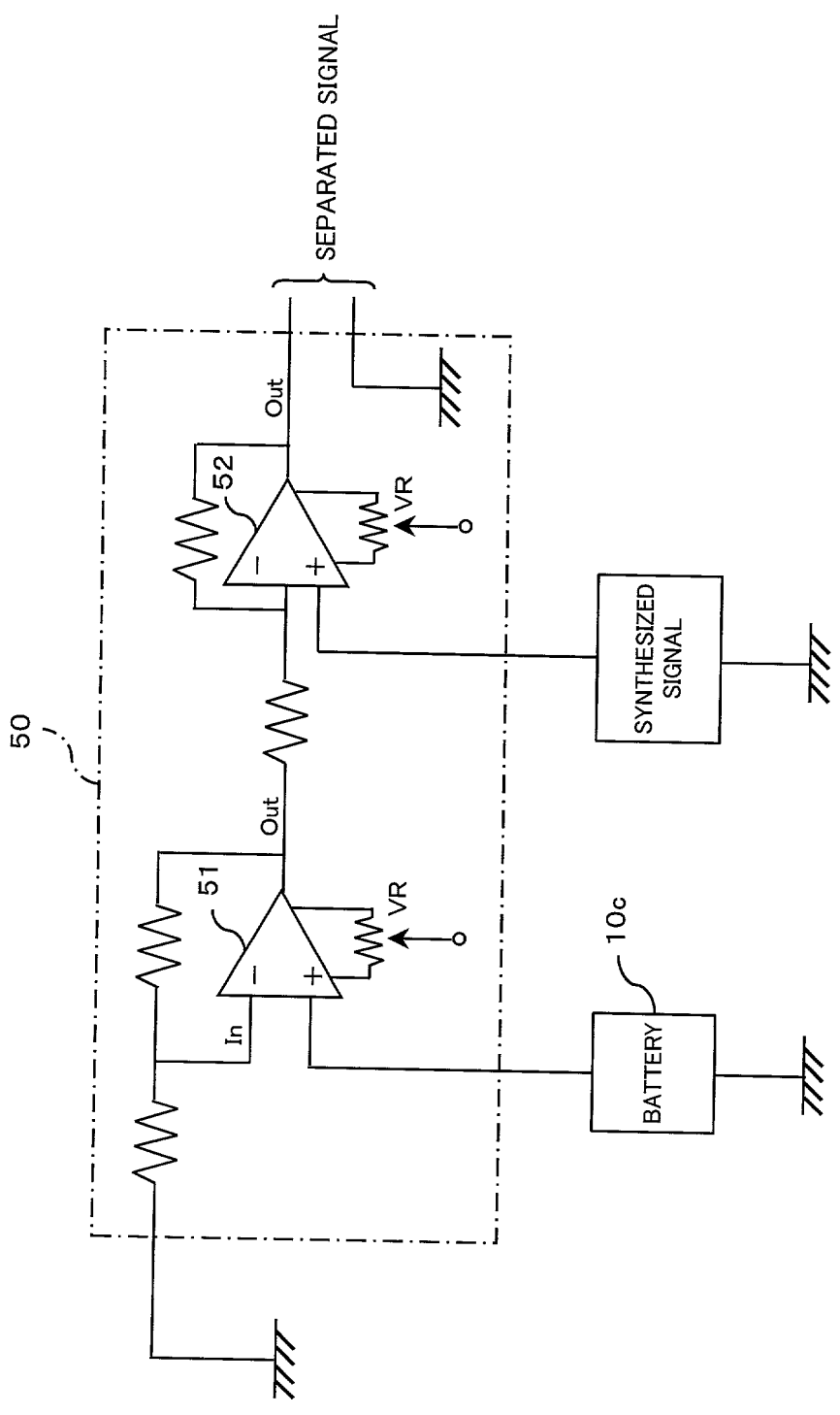


FIG. 6

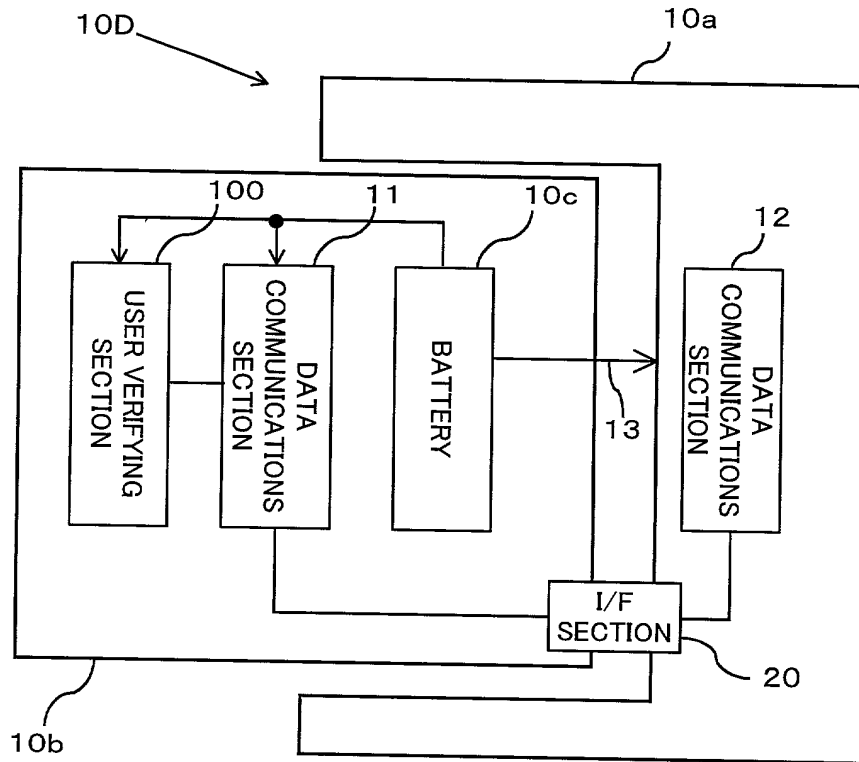


FIG. 7

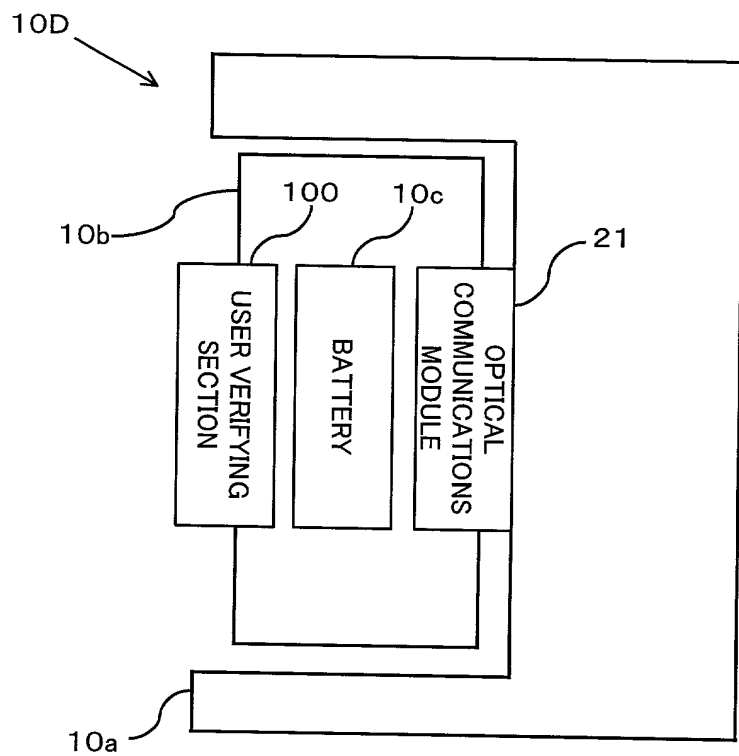


FIG. 8

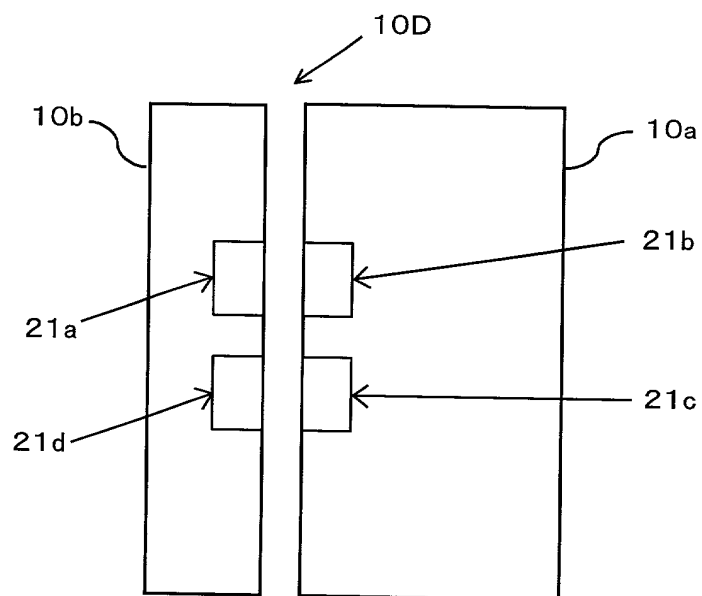






FIG. 10

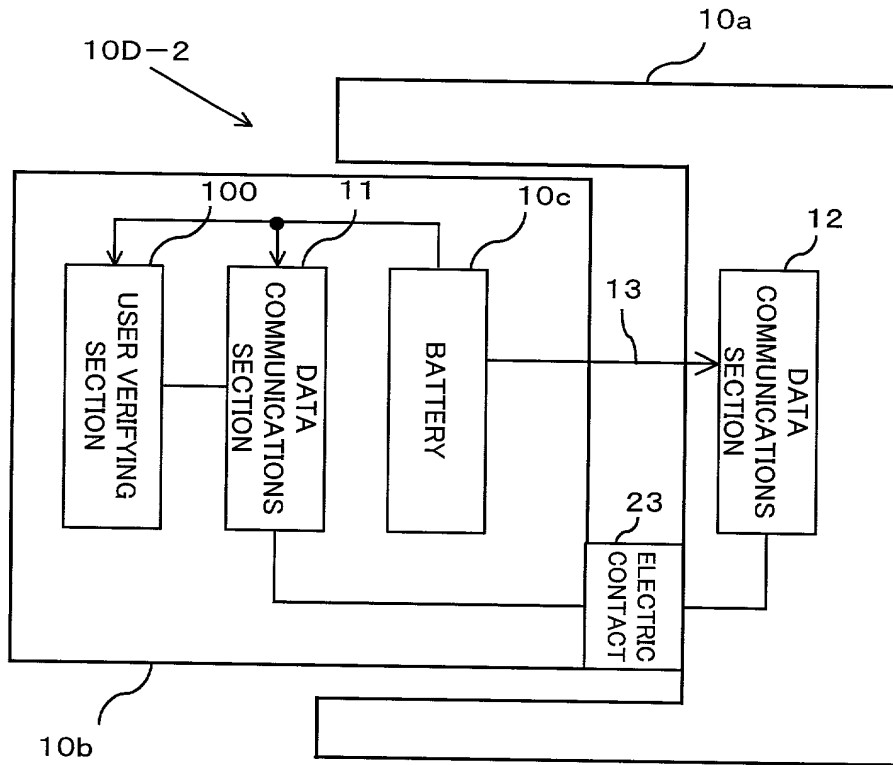


FIG. 11

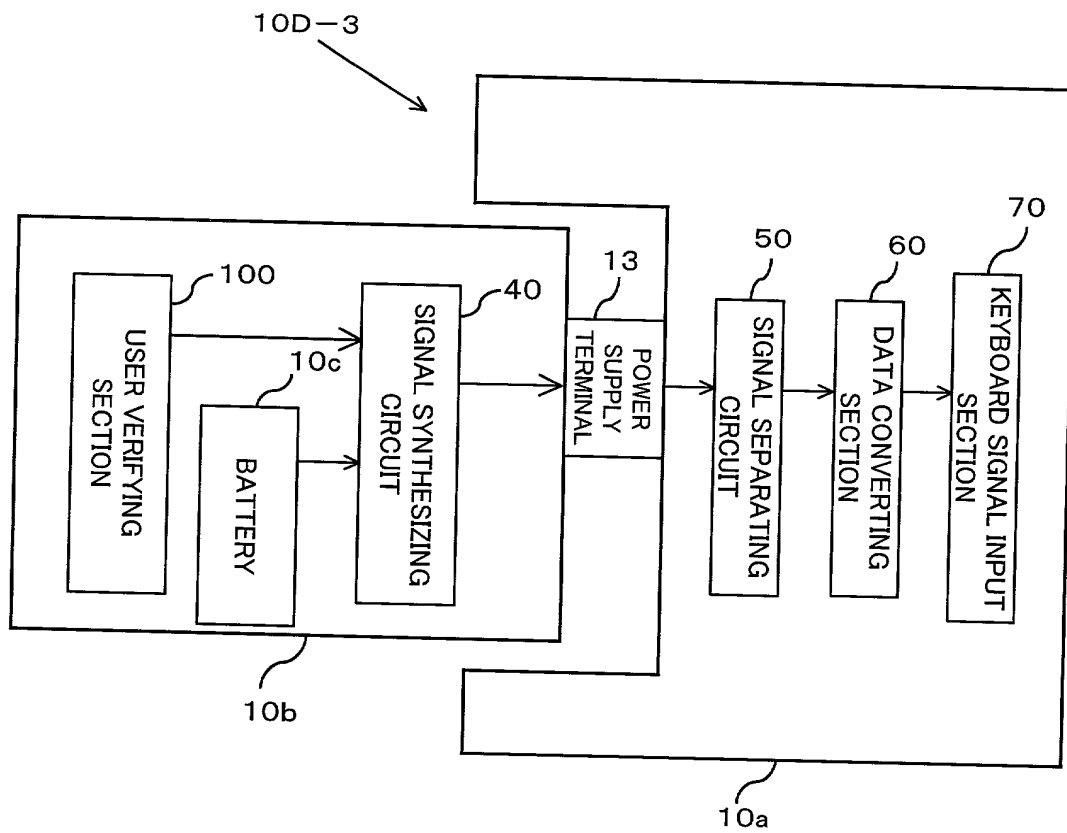


FIG. 12

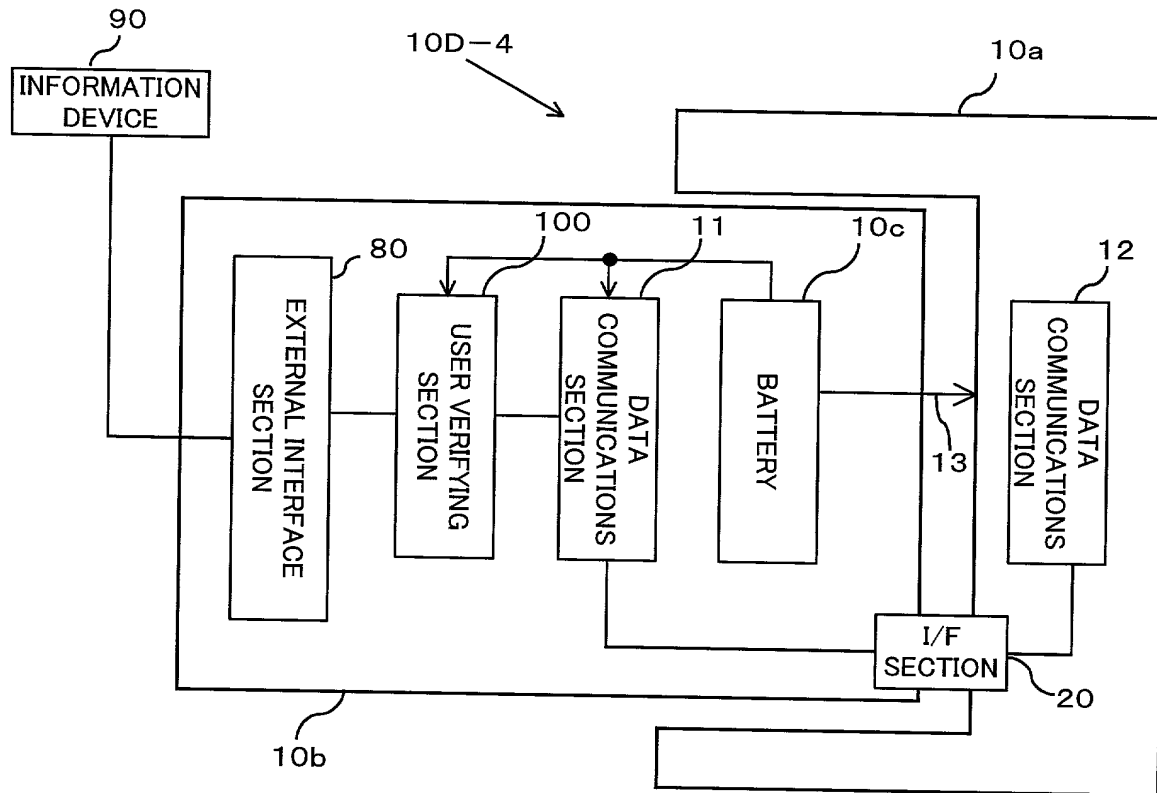


FIG. 13

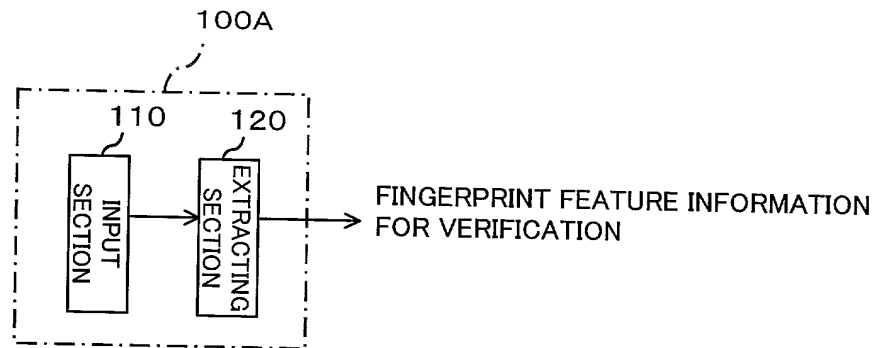


FIG. 14

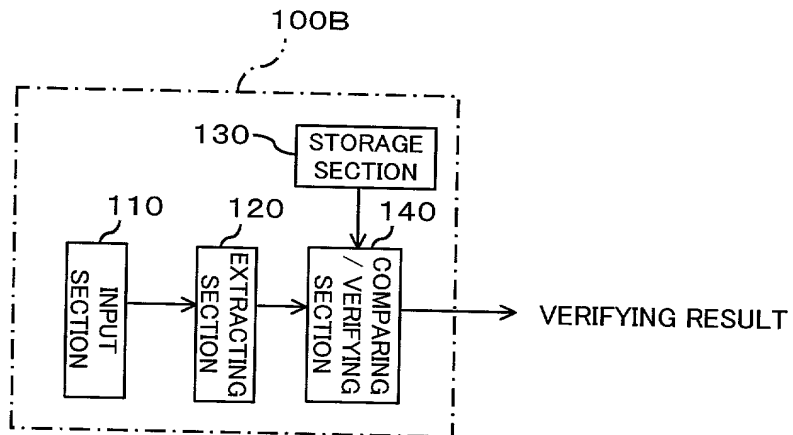


FIG. 15

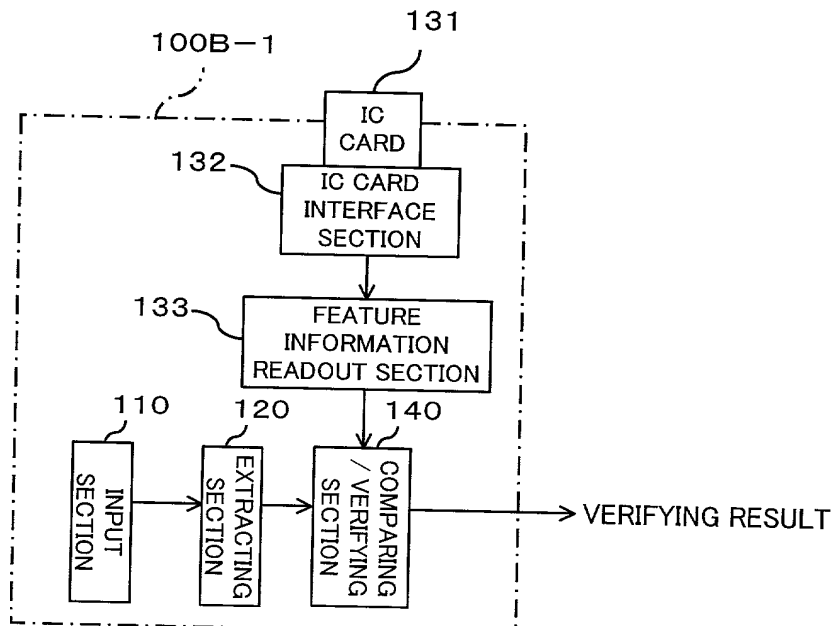


FIG. 16

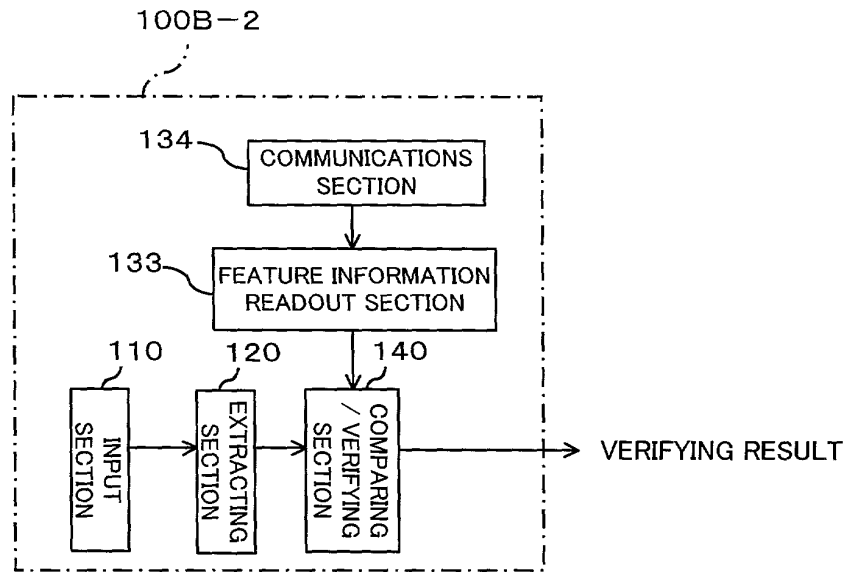


FIG. 17

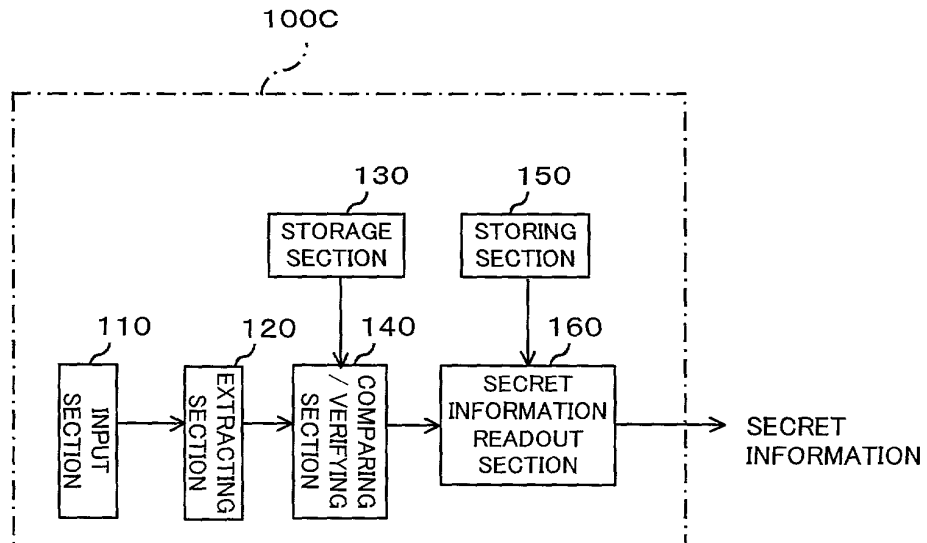


FIG. 18 is a block diagram of a cryptographic device 10D-5. The device includes a power supply terminal 13, a signal synthesizing circuit 40, a signal separating circuit 50, a data converting section 60, and a keyboard signal input section 70. The device also includes a storage section 130, a comparing/verifying section 140, an extracting section 120, a secret information readout section 160, and a battery 10c. The device is divided into sections 10a, 10b, and 10c.

FIG. 18

